

TDA7439

Three-band digitally-controlled audio processor

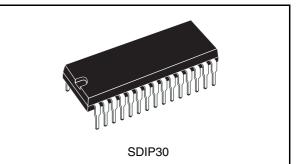
Features

- Input multiplexer
 - four stereo inputs
 - selectable input gain for optimal adaptation to different sources
- Single stereo output
- Treble, mid-range and bass control in 2-dB steps
- Volume control in 1-dB steps
- Two speaker attenuators:
 - two independent speaker controls in 1-dB steps for balance facility
 - independent mute function
- All functions are programmable via serial bus.

Description

The TDA7439 is a volume, tone (bass, mid-range and treble) and balance (left/right) processor for

Table 1. Device summary



high-quality audio applications in car-radio and Hi-Fi systems. Selectable input gain is provided. All the functions are controlled by serial bus.

The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

The TDA7439 employs BIPOLAR/CMOS technology to provide low distortion, low noise and DC stepping.

| Order code | Package | Packaging |
|------------|---------|-----------|
| TDA7439 | SDIP30 | Tube |

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1 Block diagram and pin out

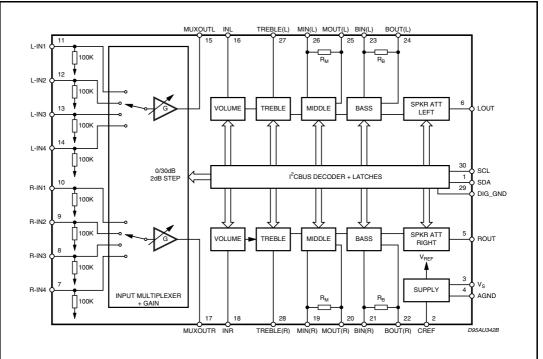
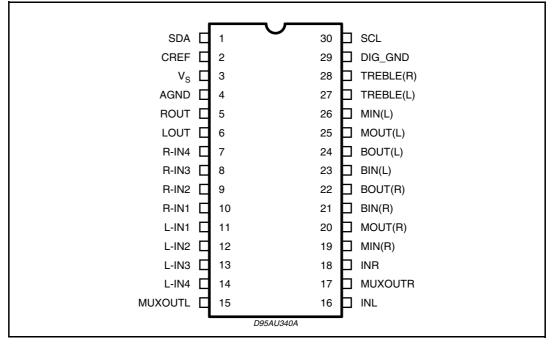


Figure 1. Block diagram

Figure 2. Pin connections





2 Electrical specifications

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|------------------|-------------------------------|------------|------|
| V _S | Operating supply voltage | 10.5 | V |
| T _{amb} | Operating ambient temperature | 0 to 70 | °C |
| T _{stg} | Storage temperature range | -55 to 150 | °C |

Table 3. Thermal data

| Symbol | Parameter | Value | Unit |
|-----------------------|----------------------------------|-------|------|
| R _{th j-pin} | Thermal resistance junction-pins | 85 | °C/W |

Table 4.Quick reference data

| Symbol | Parameter | Min | Тур | Max | Unit |
|-----------------|---|-----|------|------|----------|
| V _S | Supply voltage | 6 | 9 | 10.2 | V |
| V _{CL} | Max. input signal handling | 2 | | | V RMS |
| THD | Total harmonic distortion $V = 1 V RMS$, f = 1 kHz | | 0.01 | 0.1 | % |
| S/N | Signal to noise ratio V _{out} = 1 V RMS (mode = OFF) | | 106 | | dB |
| S _C | Channel separation f = 1 kHz | | 90 | | dB |
| | Input gain (in 2-dB steps) | 0 | | 30 | dB |
| | Volume control (in 1-dB steps) | -47 | | 0 | dB |
| | Treble control (in 2-dB steps) | -14 | | +14 | dB |
| | Middle control (in 2-dB steps) | -14 | | +14 | dB |
| | Bass control (in 2-dB steps) | -14 | | +14 | dB |
| | Balance control (in 1-dB steps) | -79 | | 0 | dB |
| | Mute attenuation | | 100 | | dB |

Table 5. shows the electrical characteristics. Refer to the test circuit in *Figure 3*, $T_{amb} = 25^{\circ}$ C, $V_{S} = 9$ V, $R_{L} = 10$ k Ω , generator resistance $R_{g} = 600 \Omega$, all controls flat (G = 0 dB), unless otherwise specified.

| Table 5. Electrical characteristic |
|------------------------------------|
|------------------------------------|

| Symbol | Parameter | Test condition | Min | Тур | Max | Unit |
|----------------|------------------|----------------|-----|-----|------|------|
| Supply | | | | | | |
| V _S | Supply voltage | | 6 | 9 | 10.2 | V |
| ۱ _S | Supply current | | 4 | 7 | 10 | mA |
| SVR | Ripple rejection | | 60 | 90 | | dB |



| Symbol | Parameter | Test condition | Min | Тур | Max | Unit |
|---------------------|---------------------------------|---|-------|----------|----------|----------|
| Input sta | ge | | | | | <u></u> |
| R _{IN} | Input resistance | | 70 | 100 | 130 | kΩ |
| V _{CL} | Clipping level | THD = 0.3% | 2 | 2.5 | | V RMS |
| S _{IN} | Input separation | The selected input is grounded through a 2.2 µF capacitor | 80 | 100 | | dB |
| G _{in_min} | Minimum input gain | | -1 | 0 | 1 | dB |
| G _{in_max} | Maximum input gain | | 29 | 30 | 31 | dB |
| G _{step} | Step resolution | | 1.5 | 2 | 2.5 | dB |
| Volume o | ontrol | | | | | |
| R _i | Volume control input resistance | | 20 | 33 | 50 | kΩ |
| C _{range} | Volume control range | | 45 | 47 | 49 | dB |
| A _{v_max} | Max. attenuation | | 45 | 47 | 49 | dB |
| A _{step} | Step resolution | | 0.5 | 1 | 1.5 | dB |
| E _A | Attenuation set error | A _V = 0 to -24 dB | -1.0 | 0 | 1.0 | dB |
| | | A _V = -24 to -47 dB | -1.5 | 0 | 1.5 | dB |
| Fm | Tue chine: curren | A _V = 0 to -24 dB | | 0 | 1 | dB |
| ΕT | Tracking error | A _V = -24 to -47 dB | | 0 | 2 | dB |
| V _{DC} | DC step | adjacent attenuation steps from 0 dB to A _{v_max} | | 0 0.5 | 3 | mV mV |
| A _{mute} | Mute attenuation | | 80 | 100 | | dB |
| Bass cor | ntrol ⁽¹⁾ | | 1 | I | | L |
| Gb | Control range | Max. boost/cut | ±12.0 | ±14.0 | ±16.0 | dB |
| B _{step} | Step resolution | | 1 | 2 | 3 | dB |
| R _B | Internal feedback resistance | | 33 | 44 | 55 | kΩ |
| Treble co | ontrol ⁽¹⁾ | | | | | |
| Gt | Control range | Max. boost/cut | ±13.0 | ±14.0 | ±15.0 | dB |
| T _{step} | Step resolution | | 1 | 2 | 3 | dB |
| Mid-rang | e control ⁽¹⁾ | ł | + | | , | μ |
| Gm | Control range | Max. boost/cut | ±12.0 | ±14.0 | ±16.0 | dB |
| M _{step} | Step resolution | | 1 | 2 | 3 | dB |
| R _M | Internal feedback resistance | | 18.75 | 25 | 31.25 | kΩ |

 Table 5.
 Electrical characteristics (continued)



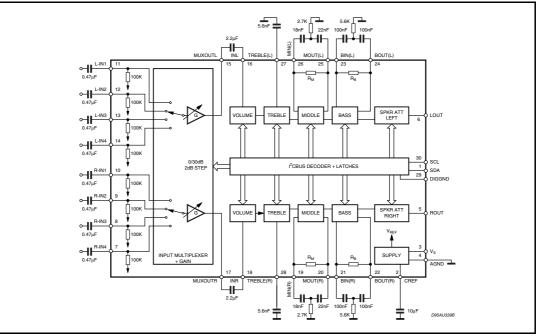
| Table 5. | | | | | | |
|--------------------|-----------------------------------|--|------|------|------|------|
| Symbol | Parameter | Test condition | Min | Тур | Мах | Unit |
| Speaker | attenuators | | Į. | | | I. |
| Crange | Control range | | 70 | 76 | 82 | dB |
| S _{step} | Step resolution | | 0.5 | 1 | 1.5 | dB |
| EA | Attenuation set error | $A_V = 0$ to -20 dB | -1.5 | 0 | 1.5 | dB |
| A | Attenuation set error | A _V = -20 to -56 dB | -2 | 0 | 2 | dB |
| V _{DC} | DC step | Adjacent attenuation steps | | 0 | 3 | mV |
| A _{mute} | Mute attenuation | | 80 | 100 | | dB |
| Audio ou | Itputs | | | | | |
| V _{CLIP} | Clipping level | d = 0.3% | 2.1 | 2.6 | | Vrms |
| RL | Output load resistance | | 2 | | | kΩ |
| R _O | Output impedance | | 10 | 40 | 70 | Ω |
| V _{OUTDC} | DC voltage level | | 3.5 | 3.8 | 4.1 | V |
| General | | | | | | |
| E _{NO} | Output noise | All gains = 0 dB; BW = 20 Hz to 20 kHz flat | | 5 | 15 | μV |
| F | Total tracking array | $A_V = 0$ to -24 dB | | 0 | 1 | dB |
| Et | Total tracking error | A _V = -24 to -47 dB | | 0 | 2 | dB |
| S/N | Signal to noise ratio | All gains 0 dB, $V_0 = 1 V RMS$ | 95 | 106 | | dB |
| S _C | Channel separation, left/right | | 80 | 100 | | dB |
| d | Distortion | $A_V = 0, V_I = 1 V RMS$ | | 0.01 | 0.08 | % |
| Bus inpu | it | | | | | • |
| V _{IL} | Input low voltage | | | | 1 | V |
| V _{IH} | Input high voltage | | 3 | | | V |
| I _{IN} | Input current | V _{IN} = 0.4 V | -5 | 0 | 5 | μA |
| Vo | Output voltage SDA acknowledge | I _O = 1.6 mA | | 0.4 | 0.8 | v |

 Table 5.
 Electrical characteristics (continued)

1. For bass, mid-range and treble response: the center frequency and the response quality can be set by the external circuitry.









3 Application suggestions

The first and the last stages are volume control blocks. The control range is 0 to -47 dB and mute for the first stage and 0 to -79 dB and mute for the last one. Both control blocks have a step resolution of 1 dB.

This very high resolution allows the implementation of systems free from any noisy acoustical effect.

The TDA7439 audio processor provides 3 bands of tone control (bass, mid-range and treble).

3.1 Tone control

3.1.1 Bass, mid-range stages

The bass and the mid-range cells have the same structure.

However, the bass cell has an internal resistor R_B of typically 44 k Ω whilst the mid-range cell has an internal resistor R_M of typically 25 k Ω .

Several filter types can be implemented by connecting external components to the bass/mid IN and OUT pins.

Typical responses are shown in *Figure 8*, *Figure 9* and *Figure 11*.

Figure 4. Bass/mid-range filter implementation

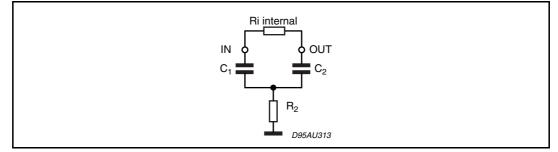


Figure 4. refers to the basic T-type band-pass filter. Starting from the filter component values (R1 (internal) and R2, C1, C2 (external)) then the centre frequency f_C , the gain Av at maximum boost and the filter Q factor are computed as follows:

$$f_{C} = \frac{1}{2 \cdot \pi \cdot \sqrt{R1 \cdot R2 \cdot C1 \cdot C2}}$$
$$A_{V} = \frac{R2C2 + R2C1 + RiC1}{R2C1 + R2C2}$$

$$\sim \sqrt{B1 \cdot B2 \cdot C1 \cdot C2}$$

$$Q = \frac{\sqrt{R11 + R2} + O(1 + O2)}{R2C1 + R2C2}$$



Transposing and solving for the external component values we get:

$$C1 = \frac{A_V - 1}{2 \cdot \pi \cdot Fc \cdot Ri \cdot Q}$$

$$C2 = \frac{Q^2 \cdot C1}{A_V - 1 - Q^2}$$

$$R2 = \frac{A_V - 1 - Q^2}{2 \cdot \pi \cdot C1 \cdot Fc \cdot (A_V - 1) \cdot Q}$$

3.1.2 Treble stage

The treble stage is a high-pass filter whose time constant is fixed by an internal resistor (25 k Ω typically) and an external capacitor connected between treble pins and ground.

Typical responses are shown in Figure 10 and Figure 11.

3.2 Pin CREF

The suggested value of 10 μ F for the reference capacitor (C_{REF}), connected to pin CREF, can be reduced to 4.7 μ F if the application requires faster power-on.

3.3 Electrical characteristics

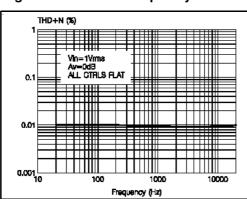
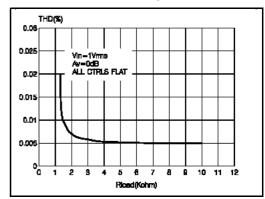


Figure 5. THD vs frequency

Figure 6. THD vs R_{LOAD}



57

57

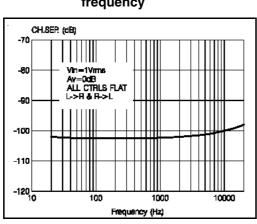


Figure 7. Channel separation vs frequency

Figure 9. Mid-range filter response

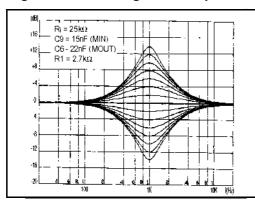


Figure 11. Typical tone response

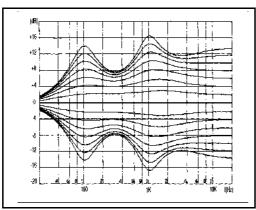


Figure 8. Bass filter response

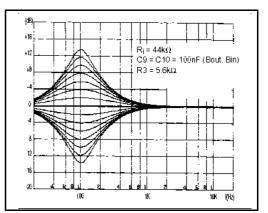
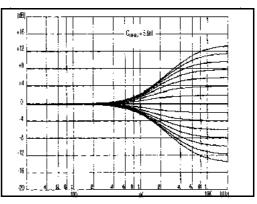


Figure 10. Treble filter response



4 I²C bus interface

Data transmission from the microprocessor to the TDA7439 and vice versa takes place through the 2-wire I²C bus interface. This consists of the data and clock lines, SDA and SCL. Pull-up resistors to the positive supply voltage must be used (there are no internal pull-ups).

4.1 Data validity

The data on the SDA line must be stable during the high period of the clock as shown in *Figure 12*. SDA is allowed to change only when SCL is low.

4.2 Start and stop conditions

As shown in *Figure 13* a start condition is a high to low transition of SDA while SCL is high. The stop condition is a low to high transition of SDA while SCL is high.

4.3 Byte format

Every byte transferred on the SDA line must contain 8 bits. The MSB is transferred first. There is also provision for an acknowledge bit to follow each byte to indicate that the data has been received.

4.4 Acknowledge

The master (μ P) puts a resistive high level on SDA during the acknowledge clock pulse (see *Figure 14*). The peripheral (audio processor) that acknowledges has to pull down (low) the SDA line during this clock pulse.

The audio processor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the high level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

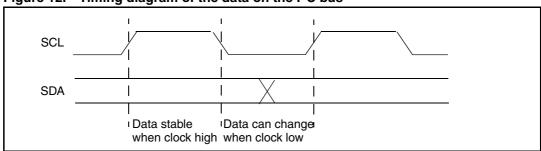
4.5 Transmission without acknowledge

Suppressing the audio processor acknowledge detection enables the μ P to use a simpler transmission: it simply waits for one clock, without checking the slave acknowledging, and then sends the new data.

This approach has, of course, less protection from transmission errors.

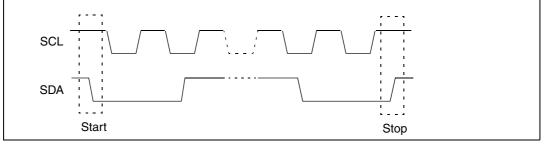


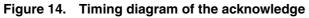
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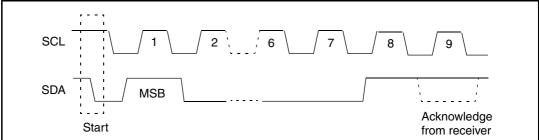












4.6 Interface protocol

The interface protocol comprises:

- a start condition (S)
- a chip-address byte, containing the TDA7439 address
- a sub-address byte including an auto address-increment bit
- a sequence of data bytes (N bytes + acknowledge)
- a stop condition (P).

Figure 15. SDA addressing and data

| CHIP ADDRESS | SUBADDRESS | DATA 1 to DATA n |
|----------------------------|-----------------------------------|------------------|
| MSB L | LSB MSB LSI | B MSB LSB |
| S 1 0 0 0 1 0 0 | 0 ACK X X X B DATA | ACK DATA ACK P |
| D96AU420 | | |
| S = Start, ACK = Acknowled | dge, B = Auto increment, P = Stop | |

5 I²C bus transmission examples

5.1 No address incrementing

The TDA7439 receives a start condition followed by the correct chip address, then a sub address with the bit B = 0 (for no address increment), then the data bytes to be sent to the sub address and finally a stop condition.

Figure 16. SDA addressing and data for B = 0

| CHIP ADD | DRESS | SUBADDRESS | DATA | |
|------------------------|-------------|-----------------------|----------|-------|
| | | | | 1 |
| MSB | LSB | MSB LSB | MSB LSE | 3 |
| S 1 0 0 0 [·] | 1 0 0 0 ACK | X X X 0 D3 D2 D1 D0 A | ACK DATA | ACK P |
| D96AU421 | | | | |

5.2 Address incrementing

The TDA7439 receives a start condition followed by the correct chip address, then a sub address with the B = 1 for address incrementing; now it is in a loop condition with an automatic increase of the sub address up to D[3:0] = 0x7. That is, the data for sub addresses from D[3:0] = 1000 (binary) to 1111 are ignored.

In *Figure 17* below, DATA1 is directed to the sub address sent (that is, D[3:0]), DATA2 is directed to the sub address incremented by 1 (that is, 1 + D[3:0]) and so forth until a stop condition is received to terminate the transmission.

| Figure 17. | SDA addressing and data for B = 1 |
|-------------|-----------------------------------|
| 1.19410 171 | |

| CHIP ADDRI | ESS | SUBAD | DRESS | DA | | |
|-------------|-----------|---------|----------------|-----|------|-------|
| | | | | | | |
| MSB | LSB | MSB | LSB | MSB | | LSB |
| S 1 0 0 0 1 | 0 0 0 ACK | X X X 1 | D3 D2 D1 D0 A0 | СК | DATA | ACK P |
| D96AU422 | | | | | | |

Table 6.Power-on-reset conditions

| Parameter | POR value |
|-----------------|-----------|
| Input selection | IN2 |
| Input gain | 28 dB |
| Volume | MUTE |
| Bass | 0 dB |
| Mid-range | 2 dB |
| Treble | 2 dB |
| Speaker | MUTE |



6 I²C bus addresses and data

6.1 Chip address byte

The TDA7439 chip address is 0x88.

6.2 Sub-address byte

The function is selected by the 4-bit sub address as given in *Table 7*. The three MSBs are not used and bit D4 selects address incrementing (B = 1) or single data byte (B = 0).

| MSB | | | | | | | LSB | Function | |
|-----|----|----|----|----|----|----|-----|------------------------|--|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Function | |
| Х | Х | Х | В | 0 | 0 | 0 | 0 | Input selector | |
| Х | Х | Х | В | 0 | 0 | 0 | 1 | Input gain | |
| Х | Х | Х | В | 0 | 0 | 1 | 0 | Volume | |
| Х | Х | Х | В | 0 | 0 | 1 | 1 | Bass gain | |
| Х | Х | Х | В | 0 | 1 | 0 | 0 | Mid-range gain | |
| Х | Х | Х | В | 0 | 1 | 0 | 1 | Treble gain | |
| Х | Х | Х | В | 0 | 1 | 1 | 0 | Speaker attenuation, R | |
| Х | Х | Х | В | 0 | 1 | 1 | 1 | Speaker attenuation, L | |

 Table 7.
 Function selection: sub-address byte

6.3 Data bytes

The function value is changed by the data byte as given in the following tables, *Table 8* to *Table 14*.

In the tables of input gain, volume and attenuation, not all values are shown. A desired intermediate value is obtained by setting the three LSBs to the appropriate value.

 Table 8.
 Input selector value (sub address 0x0)

| MSB | | | | Input multiplexer | | | | |
|-----|----|----|----|-------------------|----|----|----|-------------------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | input multiplexer |
| Х | Х | Х | Х | Х | Х | 0 | 0 | IN4 |
| Х | Х | Х | Х | Х | Х | 0 | 1 | IN3 |
| Х | Х | Х | Х | Х | Х | 1 | 0 | IN2 |
| Х | Х | Х | Х | Х | Х | 1 | 1 | IN1 |



| MSB | | | | | | | LSB | Input gain |
|-----|----|----|----|----|----|----|-----|------------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 2-dB steps |
| Х | Х | Х | Х | 0 | 0 | 0 | 0 | 0 dB |
| Х | Х | Х | Х | 0 | 0 | 0 | 1 | 2 dB |
| Х | Х | Х | Х | 0 | 0 | 1 | 0 | 4 dB |
| Х | Х | Х | Х | 0 | 0 | 1 | 1 | 6 dB |
| Х | Х | Х | Х | 0 | 1 | 0 | 0 | 8 dB |
| Х | Х | Х | Х | 0 | 1 | 0 | 1 | 10 dB |
| Х | Х | Х | Х | 0 | 1 | 1 | 0 | 12 dB |
| Х | Х | Х | Х | 0 | 1 | 1 | 1 | 14 dB |
| Х | Х | Х | Х | 1 | 0 | 0 | 0 | 16 dB |
| Х | Х | Х | Х | 1 | 0 | 0 | 1 | 18 dB |
| Х | Х | Х | Х | 1 | 0 | 1 | 0 | 20 dB |
| Х | Х | Х | Х | 1 | 0 | 1 | 1 | 22 dB |
| Х | Х | Х | Х | 1 | 1 | 0 | 0 | 24 dB |
| Х | Х | Х | Х | 1 | 1 | 0 | 1 | 26 dB |
| Х | Х | Х | Х | 1 | 1 | 1 | 0 | 28 dB |
| Х | Х | Х | Х | 1 | 1 | 1 | 1 | 30 dB |

Table 9.Input gain value (sub address 0x1)

| Table 10. | Volume value (sub address 0x2) |
|-----------|--------------------------------|
| | |

| MSB | | | | | | | LSB | Volume |
|-----|----|----|----|----|----|----|-----|------------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 1-dB steps |
| Х | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 dB |
| Х | 0 | 0 | 0 | 0 | 0 | 0 | 1 | -1 dB |
| Х | 0 | 0 | 0 | 0 | 0 | 1 | 0 | -2 dB |
| Х | 0 | 0 | 0 | 0 | 0 | 1 | 1 | -3 dB |
| Х | 0 | 0 | 0 | 0 | 1 | 0 | 0 | -4 dB |
| Х | 0 | 0 | 0 | 0 | 1 | 0 | 1 | -5 dB |
| Х | 0 | 0 | 0 | 0 | 1 | 1 | 0 | -6 dB |
| Х | 0 | 0 | 0 | 0 | 1 | 1 | 1 | -7 dB |
| Х | 0 | 0 | 0 | 1 | 0 | 0 | 0 | -8 dB |
| Х | 0 | 0 | 1 | 0 | 0 | 0 | 0 | -16 dB |
| Х | 0 | 0 | 1 | 1 | 0 | 0 | 0 | -24 dB |
| Х | 0 | 1 | 0 | 0 | 0 | 0 | 0 | -32 dB |
| Х | 0 | 1 | 0 | 1 | 0 | 0 | 0 | -40 dB |
| Х | Х | 1 | 1 | 1 | Х | Х | Х | MUTE |



| MSB | | | | | | | LSB | Bass gain |
|-----|----|----|----|----|----|----|-----|------------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 2-dB steps |
| Х | Х | Х | Х | 0 | 0 | 0 | 0 | -14 dB |
| Х | Х | Х | Х | 0 | 0 | 0 | 1 | -12 dB |
| Х | Х | Х | Х | 0 | 0 | 1 | 0 | -10 dB |
| Х | Х | Х | Х | 0 | 0 | 1 | 1 | -8 dB |
| Х | Х | Х | Х | 0 | 1 | 0 | 0 | -6 dB |
| Х | Х | Х | Х | 0 | 1 | 0 | 1 | -4 dB |
| Х | Х | Х | Х | 0 | 1 | 1 | 0 | -2 dB |
| Х | Х | Х | Х | Х | 1 | 1 | 1 | 0 dB |
| Х | Х | Х | Х | 1 | 1 | 1 | 0 | 2 dB |
| Х | Х | Х | Х | 1 | 1 | 0 | 1 | 4 dB |
| Х | Х | Х | Х | 1 | 1 | 0 | 0 | 6 dB |
| Х | Х | Х | Х | 1 | 0 | 1 | 1 | 8 dB |
| Х | Х | Х | Х | 1 | 0 | 1 | 0 | 10 dB |
| Х | Х | Х | Х | 1 | 0 | 0 | 1 | 12 dB |
| Х | Х | Х | Х | 1 | 0 | 0 | 0 | 14 dB |

 Table 11.
 Bass gain value (sub address 0x3)

| Table 12. | Mid ronge | | (ah | addraaa ()v(1) |
|-----------|------------|------------|------|----------------|
| Table 12. | wild-range | gain value | (Sub | address 0x4) |

| MSB | | | | | | | LSB | Mid-range gain |
|-----|----|----|----|----|----|----|-----|----------------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 2-dB steps |
| Х | Х | Х | Х | 0 | 0 | 0 | 0 | -14 dB |
| Х | Х | Х | Х | 0 | 0 | 0 | 1 | -12 dB |
| Х | Х | Х | Х | 0 | 0 | 1 | 0 | -10 dB |
| Х | Х | Х | Х | 0 | 0 | 1 | 1 | -8 dB |
| Х | Х | Х | Х | 0 | 1 | 0 | 0 | -6 dB |
| Х | Х | Х | Х | 0 | 1 | 0 | 1 | -4 dB |
| Х | Х | Х | Х | 0 | 1 | 1 | 0 | -2 dB |
| Х | Х | Х | Х | Х | 1 | 1 | 1 | 0 dB |
| Х | Х | Х | Х | 1 | 1 | 1 | 0 | 2 dB |
| Х | Х | Х | Х | 1 | 1 | 0 | 1 | 4 dB |
| Х | Х | Х | Х | 1 | 1 | 0 | 0 | 6 dB |
| Х | Х | Х | Х | 1 | 0 | 1 | 1 | 8 dB |
| Х | Х | Х | Х | 1 | 0 | 1 | 0 | 10 dB |
| Х | Х | Х | Х | 1 | 0 | 0 | 1 | 12 dB |
| Х | Х | Х | Х | 1 | 0 | 0 | 0 | 14 dB |



| MSB | | obio gu | | | | | LSB | Treble gain |
|-----|----|---------|----|----|----|----|-----|-------------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 2-dB steps |
| Х | Х | Х | Х | 0 | 0 | 0 | 0 | -14 dB |
| Х | Х | Х | Х | 0 | 0 | 0 | 1 | -12 dB |
| Х | Х | Х | Х | 0 | 0 | 1 | 0 | -10 dB |
| Х | Х | Х | Х | 0 | 0 | 1 | 1 | -8 dB |
| Х | Х | Х | Х | 0 | 1 | 0 | 0 | -6 dB |
| Х | Х | Х | Х | 0 | 1 | 0 | 1 | -4 dB |
| Х | Х | Х | Х | 0 | 1 | 1 | 0 | -2d B |
| Х | Х | Х | Х | Х | 1 | 1 | 1 | 0 dB |
| Х | Х | Х | Х | 1 | 1 | 1 | 0 | 2 dB |
| Х | Х | Х | Х | 1 | 1 | 0 | 1 | 4 dB |
| Х | Х | Х | Х | 1 | 1 | 0 | 0 | 6 dB |
| Х | Х | Х | Х | 1 | 0 | 1 | 1 | 8 dB |
| Х | Х | Х | Х | 1 | 0 | 1 | 0 | 10 dB |
| Х | Х | Х | Х | 1 | 0 | 0 | 1 | 12 dB |
| Х | Х | Х | Х | 1 | 0 | 0 | 0 | 14 dB |

 Table 13.
 Treble gain value (sub address 0x5)

| Table 14. | Speaker attenuation value (sub address 0x6, 0x | 7) |
|-----------|--|-------|
| 1able 14. | Speaker allenuation value (Sub audress 0x0, 0x | . () |

| MSB | | | | | LSB | Speaker attenuation | | |
|-------|----|----|----|----|-----|---------------------|----|------------|
| D7 D6 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 1-dB steps |
| Х | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 dB |
| Х | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 dB |
| Х | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 dB |
| Х | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3 dB |
| Х | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4 dB |
| Х | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 5 dB |
| Х | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 6 dB |
| Х | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 7 dB |
| Х | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 8 dB |
| Х | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 16 dB |
| Х | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 24 dB |
| Х | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 32 dB |
| Х | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 40 dB |
| Х | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 48 dB |
| Х | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 56 dB |

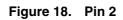


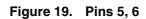
| MSB | | | Speaker attenuation | | | | | |
|-----|----|----|---------------------|----|----|----|----|------------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 1-dB steps |
| Х | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 64 dB |
| Х | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 72 dB |
| Х | 1 | 1 | 1 | 1 | Х | Х | Х | MUTE |

 Table 14.
 Speaker attenuation value (sub address 0x6, 0x7) (continued)



7 Chip input/output circuits





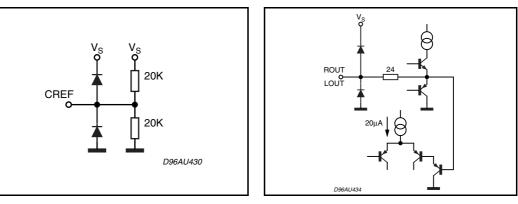
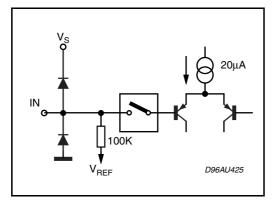


Figure 20. Pins 7, 8, 9, 10, 11, 12, 13, 14 Figure 21. Pins 15, 17



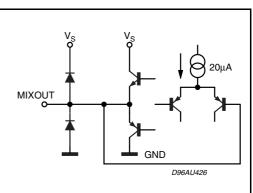


Figure 22. Pins 20, 25

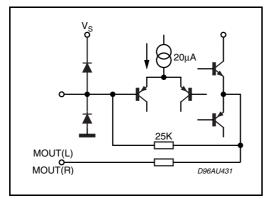


Figure 23. Pins 19, 26

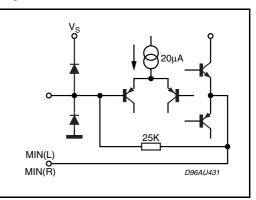
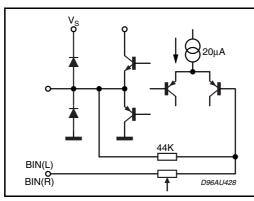
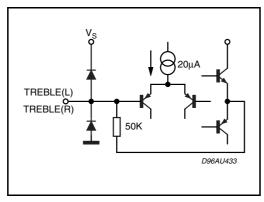




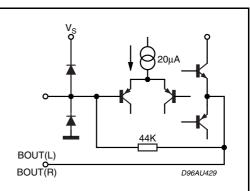
Figure 24. Pins 21, 23

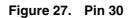


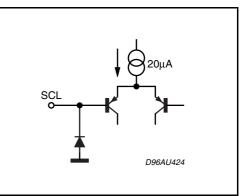


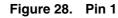


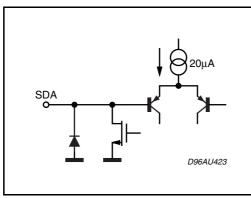




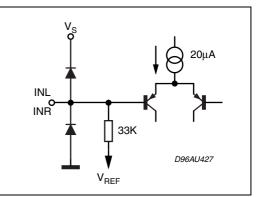












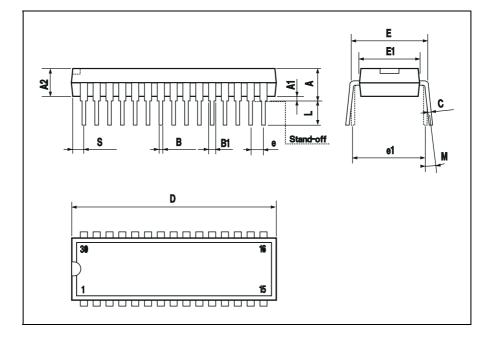


8 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

ECOPACK specifications are available at: www.st.com.

| | r | | | | | | |
|------|---------------------|-------|-------|-------|-------|-------|--|
| DIM. | | mm | | | inch | | |
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | |
| А | | | 5.08 | | | 0.20 | |
| A1 | 0.51 | | | 0.020 | | | |
| A2 | 3.05 | 3.81 | 4.57 | 0.12 | 0.15 | 0.18 | |
| В | 0.36 | 0.46 | 0.56 | 0.014 | 0.018 | 0.022 | |
| B1 | 0.76 | 0.99 | 1.40 | 0.030 | 0.039 | 0.055 | |
| С | 0.20 | 0.25 | 0.36 | 0.008 | 0.01 | 0.014 | |
| D | 27.43 | 27.94 | 28.45 | 1.08 | 1.10 | 1.12 | |
| E | 10.16 | 10.41 | 11.05 | 0.400 | 0.410 | 0.435 | |
| E1 | 8.38 | 8.64 | 9.40 | 0.330 | 0.340 | 0.370 | |
| е | | 1.778 | | | 0.070 | | |
| e1 | | 10.16 | | | 0.400 | | |
| L | 2.54 | 3.30 | 3.81 | 0.10 | 0.13 | 0.15 | |
| М | 0°(min.), 15°(max.) | | | | | | |
| S | 0.31 | | | 0.012 | | | |





9 Revision history

Table 15. Document revision history

| Date | Revision | Changes | | | | | |
|----------------|----------|---|--|--|--|--|--|
| Jan-2004 | 9 | Initial release in EDOCS DMS | | | | | |
| Jun-2004 | 10 | Modified presentation | | | | | |
| 21-Mar-2008 11 | | Updated titles to <i>Figure 9</i> and <i>Figure 10</i> Minor updates to presentation | | | | | |



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